AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An integrated circuit comprising:

a test circuit configured to generate ~~a test~~ an internal control signal ~~having a predetermined pulse width~~ in response to a control input, wherein (a) said ~~test~~ internal control signal has (i) a first pulse width when a test mode is enabled and (ii) a second pulse width when said test mode is not enabled, (b) said first pulse width is determined in response to one or more tracks process corners and ~~(ii) predicts~~ a predetermined pulse width correlating with a probability of a physical failure of said integrated circuit occurring at a future time and (c) said second pulse width is determined in response to said ~~first~~ control input.

2. (ORIGINAL) The integrated circuit according to claim 1, wherein said control input comprises a write enable input.

3. (ORIGINAL) The integrated circuit according to claim 2, wherein said control input comprises a transition of a write enable input.

4. (ORIGINAL) The integrated circuit according to claim 3, wherein said transition is from a HIGH logic level to a LOW logic level.

5. (ORIGINAL) The integrated circuit according to claim 1, wherein said first pulse width is user definable.

6. (ORIGINAL) The integrated circuit according to claim 5, wherein said first pulse width is determined in response to one or more configuration inputs.

7. (ORIGINAL) The integrated circuit according to claim 6, wherein said configuration inputs are fuse programmable.

8. (ORIGINAL) The integrated circuit according to claim 6, wherein said configuration inputs are determined by a metal masking step during fabrication.

9. (ORIGINAL) The integrated circuit according to claim 1, wherein said integrated circuit comprises a static random access memory.

10. (CURRENTLY AMENDED) The integrated circuit according to claim ~~9~~ 1, wherein said ~~test circuit is configured to predict a~~

physical failure of said integrated circuit occurs in one or more memory cells during life testing.

15. (CURRENTLY AMENDED) An integrated circuit comprising:

means for generating ~~a test~~ an internal control signal ~~having a predetermined pulse width~~ in response to a first control input, wherein (a) said internal control signal has (i) a first pulse width when in a test mode and (ii) a second pulse width when not in said test mode, (b) said first pulse width is determined in response to one or more process corners and a predetermined pulse width correlating with a probability of a physical failure in said integrated circuit occurring at a future time and (c) said second pulse width is determined in response to said first control input; and

means for ~~predicting failure of part or all of said integrated circuit~~ enabling said test mode in response to ~~said test~~ signal one or more second control inputs.

16. (CURRENTLY AMENDED) A method for ~~predicting failure of an~~ sorting integrated ~~circuit~~ circuits prior to life testing comprising the steps of:

(A) ~~entering~~ placing said integrated circuit in a test mode; and

(B) measuring a result of an operation of said integrated circuit performed in response to a ~~test~~ an internal control signal ~~having a predetermined pulse width~~ and generated on said integrated circuit in response to a control input, wherein (a) said internal control signal has (i) a first pulse width when in said test mode and (ii) a second pulse width when not in said test mode, (b) said first pulse width is determined in response to one or more process corners and a predetermined pulse width correlating with a probability of a physical failure in said integrated circuit occurring at a future time during said life testing and (c) said second pulse width is determined in response to said control input; and

~~(C) predicting said failure of said integrated circuit in response to failure of said operation.~~

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17 16
~~13~~. (ORIGINAL) The method according to claim ~~12~~, wherein said operation comprises a write operation.

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~~14~~. (CURRENTLY AMENDED) The method according to claim ~~13~~, wherein said ~~test~~ internal control signal is a write pulse presented to a start of a write path of said integrated circuit.

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15. (ORIGINAL) The method according to claim 14, wherein said write pulse has a pulse width determined by a data setup to write end time of the integrated circuit.

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16. (CURRENTLY AMENDED) The method according to claim 16
15, wherein the steps ~~(A) (C)~~ are said measurement is performed prior to said life testing.

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17. (CURRENTLY AMENDED) The method according to claim 16
15, further comprising the step of:

~~(D)~~ sorting said integrated circuits in response to said a failure of said operation.

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18. (CURRENTLY AMENDED) The method according to claim 21
17, further comprising the step of:

~~(E)~~ repairing said integrated circuit prior to said life testing.

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19. (CURRENTLY AMENDED) The method according to claim 16
15, wherein:

said operation comprises writing to a memory cell; and

said physical failure of said integrated circuit is related to a poor contact in cross-coupled latch transistors of a said memory cell.

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~~20~~. (CURRENTLY AMENDED) The method according to claim 16
~~12~~, wherein ~~step (A)~~ placing said integrated circuit in said test mode further comprises the ~~sub-steps~~ steps of:

~~(A-1)~~ applying a first high voltage to an address pin of said integrated circuit;

~~(A-2)~~ applying a second high voltage to an enable pin of said integrated circuit; and

~~(A-3)~~ removing said first high voltage from said address pin.

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~~21~~. (CURRENTLY AMENDED) The integrated circuit according to claim 1, wherein said test circuit is further configured (i) to generate present said ~~test~~ internal control signal ~~having said predetermined pulse width when in a first mode~~ to a start of a write path of said integrated circuit and (ii) to ~~pass~~ present said control input ~~as said test signal when in a second mode~~ to an end of said write path.

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~~22~~. (CURRENTLY AMENDED) The integrated circuit according to claim 11
~~21~~, wherein said test circuit is further configured to enter said ~~first~~ test mode in response to a predetermined sequence of input signals.

13. (CURRENTLY AMENDED) The integrated circuit according to claim 1, wherein said test circuit comprises:

a first circuit configured to generate said test internal control signal in response to said control input and a mode control signal; and

a second circuit configured to generate said mode control signal in response to a plurality of input signals.

14. (CURRENTLY AMENDED) The apparatus according to claim 1, wherein said physical failure is independent of said test internal control signal.